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CURRENT POSITION

The University of Electro-Communications — Tokyo, Japan
Associate Professor — Mar. 2015–Present

EDUCATION

Kyoto University — Kyoto, Japan
Ph.D., Informatics — Nov. 2007

Kyoto University — Kyoto, Japan
MS, Informatics — Mar. 2002

Kyoto University — Kyoto, Japan
BS, Engineering — Mar. 2000

WORK EXPERIENCE

Lawrence Livermore National Laboratory — Livermore, CA
Visiting Scientist and Professional — Apr. 2017–Mar. 2018

The University of Tokyo — Tokyo, Japan
Visiting Researcher — Feb. 2017–Sep. 2017

The University of Tokyo — Tokyo, Japan
Assistant Professor — Apr. 2011–Feb. 2015

Tokyo University of Agriculture and Technology — Tokyo, Japan
Project Assistant Professor — Jan. 2008–Mar. 2011

Kyoto University — Kyoto, Japan
Research Associate — Apr. 2005–Dec. 2007

TEACHING EXPERIENCE

The University of Electro-Communications Tokyo, Japan

- *Mathematical Information Science Laboratory II/Computer Science Laboratory II* (CPU cache simulation), Second term 2018–Present
- *Logic Circuit Design,* First term 2018–Present
- *Parallel Processing II/High Performance Computing II*, Second term 2015–Present
- *Mathematical Information Science Laboratory I/Computer Science Laboratory I* (Logic circuit and Verilog-HDL), First term 2016
- *Elements of Information Systems Fundamentals I* (Computer architecture), First term 2015

The University of Tokyo Tokyo, Japan

- *Mathematical Engineering and Information Physics Laboratory I* (Logic circuit and Verilog-HDL)*,* First term 2013–2014
- *Information System Design Laboratory* (C programming), First term 2011–2014

RESEARCH INTERESTS

Computer architecture High performance computing System software Embedded systems

SELECTED PUBLICATIONS

- **S. Miwa**, M. Ishihara, H. Yamaki, H. Honda, and M. Schulz, Footprint-Based DIMM Hotplug, IEEE Transactions on Computers, Vol. 69, Issue 2, pp.172–184, Feb. 2020 *(Featured Paper in the February 2020 issue)*.
- H. Yamaki, H. Nishi, **S. Miwa,** and H. Honda, Data Prediction for Response Flows in Packet Processing Cache, In Proceedings of the 2018 55th ACM/EDAC/IEEE Design Automation Conference (DAC), No. 110, 6 pages, Jul. 2018 *(acceptance rate: 158/747=21%)*.
- **S. Miwa**, and H. Nakamura, Profile-Based Power Shifting in Interconnection Networks with On/Off Links, In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis (SC15), pp.37:1–37:11, Nov. 2015 *(acceptance rate: 79/358=22%)*.
- **S. Miwa**, and C. R. Lefurgy, Evaluation of Core Hopping on POWER7, ACM SIGMETRICS Performance Evaluation Review, Special Issue on Greenmetrics 2014, pp. 11–16, 2014 (also appeared in the 2014 GreenMetrics Workshop, 6 pages, Jun. 2014).
- Y. He, H. Sasaki, **S. Miwa**, and H. Nakamura, McRouter: Multicast within a Router for High Performance Network-on-Chips, In Proceedings of the 22nd International Conference on Parallel Architectures and Compilation Techniques (PACT'13), pp.319–329, Sep. 2013 *(acceptance rate: 36/208=17%)*.

SELECTED INVITED TALKS

- Variation of GPU Power in Supercomputing Systems, George Washington University, Washington, DC, USA, Sep. 2019.
- Energy-Efficient Computers with Increased Hardware Resources, the 78th National Convention of Information Processing Society of Japan, Mar. 2016 (in Japanese).
- Network and Memory Power Management in High Performance Computing Systems, IBM Austin Research Labs, Austin, TX, USA, Nov. 2015.
- Power Shifting between Networks and CPUs in HPC System, JST/CREST International Symposium on Post Petascale System Software, Dec. 2014.
- Power Management for Exascale Computing, IBM Austin Research Labs, Austin, TX, USA, Feb. 2014.

RESEARCH GRANTS

- Development of Innovative Frameworks for Application Analysis in Post-Peta Scale Systems, 20H04193, Grant-in-Aid for Scientific Research, Japan Society for the Promotion of Science, 14,320,000 JPY, principal investigator, Apr. 2020–Present.
- Resource Manager in Next-Generation Massively Parallel Processing Environments, Research Grant, KDDI Foundation, 3,000,000 JPY, principal investigator, Apr. 2020–Present.
- A Study of Performance Evaluation and Memory Models of AI Applications on High Performance Computing Systems, KIOXIA Corp., 2,200,000 JPY, principal investigator, Jul. 2019–Present.
- A Study of Profile Prediction for MPI Parallel Applications Executed on Massively Parallel Processing Environments, K30-XXIII-524, Research Grant, Kayamori Foundation of Informational Science Advancement, 800,000 JPY, principal investigator, Nov. 2018–Present *(acceptance rate: 21/162=13%)*.
- A Study of Ultrascaled Nanocarbon Processor Architecture, 18K19778, Grant-in-Aid for Scientific Research, Japan Society for the Promotion of Science, 6,240,000 JPY, principal investigator, Apr. 2018–Present *(acceptance rate: 1,466/12,141=12%)*.
- Power Management Framework for Post-Peta Scale Systems, Core Research for Evolutionary Science and Technology, Japan Science and Technology Agency, 223,254,000 JPY, co-investigator (PI: Professor Masaaki Kondo), Oct. 2012–Mar. 2018.
- Development of Fundamental Technology for Normally-off Computing, Toshiba Corp., 1,000,080 JPY, principal investigator, May 2015–Feb. 2016.
- A Study of Heat-Spread-Aware Processors, R24700044, Grant-in-Aid for Scientific Research, Japan Society for the Promotion of Science, 4,420,000 JPY, principal investigator, Apr. 2012–Mar. 2014 *(acceptance rate: 6,255/20,867=30%)*.

AWARDS (FOR ME)

- *Best Paper Award for Computers Track in the 2019 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing,* Aug. 2019.
- *Best Paper Award in the 2010 Embedded System Symposium*, Oct. 2010.
- *Second Place in the free programming track of the 2010 GPU Challenge*, May 2010.
- *Best Poster Award in the 2008 Symposium on Advanced Computing Systems and Infrastructures*, Jun. 2008.
- *Student Encouragement Award received from Kansai-Section Convention of Information Processing Society of Japan*, Oct. 2003.

AWARDS (FOR GRADUATES AND UNDERGRADUATES)

- K. Tanaka, *IPSJ Yamashita SIG Research Award,* 2019.
- K. Tanaka, *IEEE CEDA All Japan Joint Chapter Design Gaia Best Poster Award*, Dec. 2018.
- K. Tanaka, *Third Place in the undergraduate category at MICRO51 ACM Student Research Competition*, Oct. 2018.
- Y. He, his Ph.D. thesis is selected as *one of the best papers recommended by SIG (Special Interest Group) of System Architecture in IPSJ (Information Processing Society of Japan)*, Jul. 2014.
- A. Ohta, his Ph.D. thesis is selected as *one of the best papers recommended by SIG of Embedded Systems in IPSJ*, Jul. 2013.
- A. Ohta, *Encouragement Award in the Field of Computer Science of IPSJ*, Oct. 2010.

SELECTED PROFESSIONAL ACTIVITIES

Track Chair

- IEEE International Symposium on Embedded Multicore/Many-core System-on-Chip (MCSoC), 2018–2020.

Technical Program Committees

- IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid), 2018–2019.
- International Conference on Parallel Processing (ICPP), 2018.
- IEEE International Conference on Computer Design (ICCD), 2014–2015.

Editorial Boards

- IEICE (Institute of Electronics, Information and Communication Engineers) Transactions on Information and Systems, Jun. 2015–May 2019.

- IPSJ Magazine, Apr. 2010–Mar. 2016.
- IPSJ Transactions on Advanced Computing Systems, Apr. 2011–Mar. 2015, Apr. 2020–Present.
- IPSJ Journal of Information Processing, Jun. 2009–May 2013.

External Reviewers

- ACM/EDAC/IEEE Design Automation Conference (DAC), 2014.
- ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2012.
- International Conference for High Performance Computing, Networking, Storage and Analysis (SC), 2011–2012.
- ACM International Conference on Supercomputing (ICS), 2008.

Others

- Evaluation committee member of Energy-Saving Project, New Energy and Industrial Technology Development Organization, Apr. 2016–Present.

FULL PUBLICATIONS LIST

Journal Articles

- **S. Miwa**, M. Ishihara, H. Yamaki, H. Honda, and M. Schulz, Footprint-Based DIMM Hotplug, IEEE Transactions on Computers, Vol. 69, Issue 2, pp.172-184, 2020 *(Featured Paper in the February 2020 issue)*.
- Y. He, M. Kondo, T. Nakada, H. Sasaki, **S. Miwa**, and H. Nakamura, A Runtime Optimization Selection Framework to Realize Energy Efficient Network-on-Chip, IEICE Transactions on Information and Systems, Vol. E99-D, No. 5, pp. 1–10, 2016.
- **S. Miwa**, S. Aita, Y. Ajima, T. Shimizu, A. Asato, and H. Nakamura, Power/Performance Evaluation of EEE in Real HPC Environment, IPSJ Transactions on Advanced Computing Systems, Vol. 7, No. 4, pp. 67–83, 2014 (in Japanese).
- **S. Miwa**, and C. R. Lefurgy, Evaluation of Core Hopping on POWER7, ACM SIGMETRICS Performance Evaluation Review, Special Issue on Greenmetrics 2014, pp. 11–16, 2014 (also appeared in the 2014 GreenMetrics Workshop, 6 pages, Jun. 2014).
- E. Arima, T. Komoda, T. Nakada, **S. Miwa**, H. Noguch, K. Nomura, K. Abe, S. Fujita, and H. Nakamura, Analysis of Performance Required for STT-MRAM Last Level Caches Under Low CPU Load, IEICE Transactions on Electronics, Communications and Computer Sciences, Vol. J97-A, No. 10, pp. 629–647, 2014 (in Japanese).
- T. Nakada, K. Okamoto, T. Komoda, **S. Miwa**, Y. Sato, H. Ueki, M. Hayashikoshi, T. Shimizu, and H. Nakamura, Design Aid of Multi-core Embedded Systems with Energy Model, IPSJ Transactions on Advanced Computing Systems, Vol. 7, No. 3, pp. 37–46, 2014.
- **S. Miwa**, T. Inoue, and H. Nakamura, Area-Efficient Microarchitecture for Reinforcement of Turbo Mode, IEICE Transactions on Information and Systems, Vol. E97-D, No. 5, pp. 1196–1210, 2014.
- **S. Miwa**, S. Aita, and H. Nakamura, Performance Estimation of High Performance Computing Systems with Energy Efficient Ethernet Technology, Journal of Computer Science – Research and Development, Vol. 29, Issue 3-4, pp. 161-169, 2014 (also appeared in International Conference on Energy-Aware High Performance Computing (EnA-HPC'13), 8 pages, Sep. 2013).
- E. Arima, T. Komoda, T. Nakada, **S. Miwa**, and H. Nakamura, Lost Data Prefetching to Reduce Performance Degradation Caused by Powering Off Caches, IPSJ Transactions on Advanced Computing Systems, Vol. 6, No. 3, pp.118–130, 2013 (in Japanese).
- K. Kim, S. Takeda, **S. Miwa**, and H. Nakamura, Evaluation of a New Power-Gating Scheme Utilizing Data Retentiveness on Caches, IEICE Transaction on Electronics, Communications and Computer Sciences, Vol. E95-A, No. 12, pp. 2301–2308, Dec. 2012.
- P. Waskito, **S. Miwa**, Y. Mitsukura and H. Nakajo, Evaluation of GPU-based Empirical Mode

Decomposition for Off-line Analysis, IEICE Transactions on Information and Systems, Vol. E94-D, No. 12, pp. 2328–2337, Dec. 2011.

- A. Ohta, **S. Miwa** and H. Nakajo, Proposal of a Hardware Scheme for Java Acceleration on Android Devices, IPSJ Transactions on Advanced Computing Systems, Vol. 4, No. 2, pp.115–132, 2011 (in Japanese).
- J. Yao, **S. Miwa**, H. Shimada and S. Tomita, A Fine-Grained Runtime Power/Performance Optimization Method for Processors with Adaptive Pipeline Depth, Journal of Computer Science and Technology, Vol. 26, No. 2, pp. 292–301, 2011.
- **S. Miwa**, P. Zhang, H. Yokoyama, Y. Horibe and H. Nakajo, Area-efficient Register Map Table Using a Cache, IPSJ Transactions on Advanced Computing Systems, Vol. 3, No. 3, pp. 44–55, 2010 (also appeared in the 2010 Symposium on Advanced Computing Systems and Infrastructures, pp. 329–338, May 2010) (in Japanese).
- J. Yao, K. Ogata, H. Shimada, **S. Miwa**, H. Nakashima and S. Tomita, An Instruction Scheduler for Dynamic ALU Cascading Adoption, IPSJ Transactions on Advanced Computing Systems, Vol. 2, No. 2, pp.30–47, 2009.
- Y. Ogasawara, **S. Miwa** and H. Nakajo, Dynamic Switch Strategies of Accessing L1/L2 Cache for an SMT Processor, IPSJ Transactions on Advanced Computing Systems, Vol. 2, No. 3, pp. 12–25, 2009 (also appeared in the 2009 Symposium on Advanced Computing Systems and Infrastructures, pp. 379–388, May 2009) (in Japanese).
- J. Yao, **S. Miwa**, H. Shimada and S. Tomita, A Dynamic Control Mechanism for Pipeline Stage Unification by Identifying Program Phases, IEICE Transactions on Information and Systems, Vol. E91-D, No. 4, pp. 1010–1022, April 2008.
- **S. Miwa**, H. Ichibayashi, H. Irie, M. Goshima and S. Tomita, Low-complexity Operand Bypass Using Small RAM, IPSJ Transactions on Advanced Computing Systems, Vol. 48, No. SIG13, pp. 58–69, 2007 (also appeared in the 2007 Symposium on Advanced Computing Systems and Infrastructures, pp. 265–274, May 2007) (in Japanese).
- **S. Miwa**, T. Fukuyama, H. Shimada, M. Goshima, Y. Nakashima, S. Mori and S. Tomita, Branch Filtering Mechanism with Path Trace, IPSJ Transactions on Advanced Computing Systems, Vol. 47, No. SIG12, pp.108–118, 2006 (also appeared in the 2006 Symposium on Advanced Computing Systems and Infrastructures, pp. 315–323, May 2006) (in Japanese).

Conferences

- G. Georgakoudis, N. Jain, T. Ono, K. Inoue, **S. Miwa**, and A. Bhatele, Evaluating the Impact of Energy Efficient Networks on HPC Workloads, 26th IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC), 10 pages, Dec. 2019 *(acceptance rate: 39/173=23%)*.

- Y. Inouchi, H. Yamaki, **S. Miwa**, and T. Tsumura, Functionally-Predefined Kernel: a Way to Reduce CNN Computation, The 2019 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing (PacRim 2019), 6 pages, Aug. 2019 *(Best paper award for computers track: 1/27=3.7%).*
- K. Tanaka, H. Yamaki, **S. Miwa**, and H. Honda, Multi-Level Packet Processing Caches, The 2019 IEEE Symposium on Low-Power and High-Speed Chips and Systems (COOL Chips 22), 3 pages, Apr. 2019.
- K. Tanaka, H. Yamaki, **S. Miwa**, and H. Honda, Optimizing Memory Hierarchy within an Internet Router for High-Throughput and Energy-Efficient Packet Processing, ACM Student Research Competition (in conjunction with the 51st Annual ACM/IEEE International Symposium on Microarchitecture (MICRO-51), poster presentation), Oct. 2018 *(won 3rd place in the undergraduate category)*.
- H. Yamaki, H. Nishi, **S. Miwa**, and H. Honda, Data Prediction for Response Flows in Packet Processing Cache, In Proceedings of the 2018 55th ACM/EDAC/IEEE Design Automation Conference (DAC), No. 110, 6 pages, Jul. 2018 *(acceptance rate: 158/747=21%)*.
- Miyoshi, **S. Miwa**, K. Inoue, and M. Kondo, Run-Time DFS/DCT Optimization for Power-Constrained HPC Systems, the International Conference on High Performance Computing in Asia-Pacific Region (HPC Asia 2018, poster presentation), Jan. 2018.
- S. Shindo, M. Ohba, T. Tsumura, and **S. Miwa**, Evaluation of Task Mapping on Multicore Neural Network Accelerators, In Proceedings of the 4th International Workshop on Computer Systems and Architectures, pp. 415–421, Nov. 2016.
- M. Ohba, **S. Miwa**, S. Shindo, T. Tsumura, H. Yamaki, and H. Honda, Initial Study of Reconfigurable Neural Network Accelerators, In Proceedings of the 7th International Workshop on Advances in Networking and Computing (poster presentation), pp. 707–709, Nov. 2016.
- **S. Miwa**, and H. Nakamura, Profile-Based Power Shifting in Interconnection Networks with On/Off Links, In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis (SC15), pp.37:1–37:11, Nov. 2015 *(acceptance rate: 79/358=22%)*.
- **S. Miwa**, and H. Honda, Memory Hotplug for Energy Savings of HPC systems, the International Conference for High Performance Computing, Networking, Storage and Analysis (SC15, poster presentation), Nov. 2015 *(acceptance rate: 112/253=44%, best poster award finalists: 7/253=3%)*.
- E. Arima, H. Noguchi, T. Nakada, **S. Miwa**, S. Takeda, S. Fujita, and H. Nakamura, Immediate Sleep: Reducing Energy Impact of Peripheral Circuits in STT-MRAM Caches, In Proceedings of the 33rd IEEE International Conference on Computer Design (ICCD'15), pp.157–164, Oct.

2015 *(acceptance rate: 83/269=31%)*.

- Y. He, M. Kondo, T. Nakada, H. Sasaki, **S. Miwa**, and H. Nakamura, Runtime Multi-Optimizations for Energy Efficient On-chip Interconnections, In Proceedings of the 33rd IEEE International Conference on Computer Design (ICCD'15, poster presentation), pp. 484–487, Oct. 2015.
- E. Arima, **S. Miwa**, T. Nakada, S. Takeda, H. Noguchi, S. Fujita, and H. Nakamura, Subarray Level Power-Gating in STT-MRAM Caches to Mitigate Energy Impact of Peripheral Circuits, the 2015 52nd ACM/EDAC/IEEE Design Automation Conference (DAC), Work-in-Progress Session (poster presentation), Jun. 2015.
- T. Nakada, T. Shigematsu, T. Komoda, **S. Miwa**, Y. Sato, H. Ueki, M. Hayashikoshi, T. Shimizu, and H. Nakamura, Data-aware Power Management for Periodic Real-time Systems with Non-Volatile Memory, In Proceedings of the 3rd IEEE Nonvolatile Memory Systems and Applications Symposium (NVMSA'14), 6 pages, Aug. 2014.
- E. Arima, T. Nakada, **S. Miwa**, S. Takeda, H. Noguchi, S. Fujita, and H. Nakamura, Fine-Grain Power-Gating on STT-MRAM Peripheral Circuits with Locality-aware Access Control, the Memory Forum (in conjunction with the 41st International Symposium on Computer Architecture (ISCA-41)), 5 pages, Jun. 2014.
- T. Komoda, S. Hayashi, T. Nakada, **S. Miwa**, and H. Nakamura, Power Capping of CPU-GPU Heterogeneous Systems through Coordinating DVFS and Task Mapping, In Proceedings of the 31st IEEE International Conference on Computer Design (ICCD'13), pp.349–356, Oct. 2013 *(acceptance rate: 56/223=25%)*.
- T. Nakada, **S. Miwa**, K. Yano, and H. Nakamura, Performance Modeling for Designing NoC-based Multiprocessors, In Proceedings of the 2013 IEEE International Symposium on Rapid System Prototyping (RSP'13), pp.30–36, Oct. 2013.
- T. Komoda, N. Maruyama, **S. Miwa**, and H. Nakamura, Integrating Multi-GPU Execution in an OpenACC Compiler, In Proceedings of the 42nd International Conference on Parallel Processing (ICPP'13), pp.260–269, Oct. 2013 *(acceptance rate: 59/193=31%)*.
- Y. He, H. Sasaki, **S. Miwa**, and H. Nakamura, McRouter: Multicast within a Router for High Performance Network-on-Chips, In Proceedings of the 22nd International Conference on Parallel Architectures and Compilation Techniques (PACT'13), pp.319–329, Sep. 2013 *(acceptance rate: 36/208=17%)*.
- Y. He, H. Sasaki, **S. Miwa**, and H. Nakamura, Predict-more Router: A Low Latency NoC Router with More Route Predictions, In Proceedings of the 3rd Workshop on Communication Architecture for Scalable Systems (CASS'13), pp. 842–850, May 2013.
- H. Noguchi, K. Nomura, K. Abe, S. Fujita, E. Arima, K. Kim, T. Nakada, **S. Miwa**, and H. Nakamura, D-MRAM Cache: Enhancing Energy Efficiency with 3T-1MTJ DRAM/MRAM

Hybrid Memory, In Proceedings of the 2013 Design, Automation & Test in Europe (DATE'13), pp.1813–1818, Mar. 2013 *(acceptance rate: 206/829=25%)*.

- E. Arima, T. Komoda, **S. Miwa**, H. Noguchi, K. Nomura, K. Abe, S. Fujita, and H. Nakamura, Comparison of Leak Reduction Techniques for Last Level Caches under OS Power Management, In Proceedings of the 25th Workshop on Circuit and Systems, pp. 402–407, Jul. 2012 (in Japanese).
- S. Takeda, **S. Miwa**, K. Usami, and H. Nakamura, Stepwise Sleep Depth Control for Run-Time Leakage Power Saving, In Proceedings of the 2012 Great Lakes Symposium on VLSI (GLSVLSI'12), pp.233–238, May 2012 *(acceptance rate: 41/144=28%)*.
- K. Kim, S. Takeda, **S. Miwa** and H. Nakamura, A Novel Power-Gating Scheme Utilizing Data Retentiveness on Caches, In Proceedings of the 2012 Great Lakes Symposium on VLSI (GLSVLSI'12, poster presentation), pp. 91–94, May 2012.
- T. Komoda, **S. Miwa** and H. Nakamura, Communication Library to Overlap Computation and Communication for OpenCL Application, In Proceedings of the 17th International Workshop on High-Level Parallel Programming Models and Supportive Environment (HIPS'12), pp. 560–566, May 2012.
- S. Takeda, **S. Miwa**, K. Usami and H. Nakamura, Efficient Leakage Power Saving by Sleep Depth Controlling for Multi-mode Power Gating, In Proceedings of the 13th International Symposium on Quality Electronic Design (ISQED'12), pp. 627–634, Mar 2012.
- H. Horibe, **S. Miwa**, R. Shioya, M. Goshima, and H. Nakajo, Selective Cache Line Allocation with Load/Store Instruction Address, In Proceedings of the 2011 Symposium on Advanced Computing Systems and Infrastructures, pp. 316–323, May 2011 (in Japanese).
- P. Waskito, **S. Miwa**, Y. Mitsukura and H. Nakajo, Parallelizing Hilbert-Huang Transform on GPU, In Proceedings of the 2nd Workshop on Ultra Performance and Dependable Acceleration Systems (UPDAS'10), pp. 184–190, Nov. 2010.
- Ohta, **S. Miwa**, and H. Nakajo, Dalvik Accelerator: A Framework for High-Performance Execution of Java Applications on Android Devices, In Proceedings of the 2010 Embedded System Symposium, pp. 13–22, Oct. 2010 (in Japanese) *(Best Paper Award)*.
- H. Yokoyama, Y. Horibe, P. Zhang, **S. Miwa** and H. Nakajo, An Effective Replacement Policy Focusing on Lifetime of a Cache Line, In Proceedings of the 2010 International Conference on Computer Design (CDES'10), pp. 146–152, Jul. 2010.
- P. Waskito, **S. Miwa**, Y. Mitsukura, and H. Nakajo, Parallelizing Hilbert-Huang Transform and its Acceleration with GPU, In Proceedings of the 2010 Symposium on Advanced Computing Systems and Infrastructures (poster presentation), pp. 139–140, May 2010 (in Japanese) *(won 2nd place in the free programming track of the 2010 GPU Challenge)*.
- Y. Horibe, **S. Miwa**, R. Shioya, M. Goshima, and H. Nakajo, Improving Efficiency of Cache

Capacity by Selective Cache Line Allocation, In Proceedings of the 2010 Symposium on Advanced Computing Systems and Infrastructures (poster presentation), pp. 121–122, May 2010 (in Japanese).

- Ohta, T. Motegi, **S. Miwa**, and H. Nakajo, A MIPS-Simulator-Based Framework for Evaluating Dalvik Accelerators, In Proceedings of the 2010 Symposium on Advanced Computing Systems and Infrastructures (poster presentation), pp. 113–114, May 2010 (in Japanese).
- M. Nakanishi, Y. Mitsukura, T. Tanaka, **S. Miwa** and H. Nakajo, Extraction of horns in a noisy environment by EMD, In Proceedings of the 2010 International Workshop on Nonlinear Circuits and Signal Processing (NCSP'10), pp. 333–336, Mar. 2010.
- Y. Ogasawara, P. Waskito, **S. Miwa** and H. Nakajo, Dynamic Switching Techniques of Accessing L1/L2 Cache on an SMT Processor, In Proceedings of the 2009 International Conference on Computer Design (CDES'09), pp. 171–177, Jul. 2009.
- J. Yao, H. Shimada, K. Ogata, **S. Miwa** and S. Tomita, Improving Effectiveness of Pipeline Stage Unification via ALU Cascading, In Proceedings of the 12th IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips XII), pp.423–436, Apr. 2009.
- **S. Miwa**, H. Ichibayashi, H. Irie, M. Goshima, H. Nakajo, and S. Tomita, Low-Complexity Bypass Network Using Small RAM, In Proceedings of the 2008 International Conference on Computer Design (CDES'08), pp. 153–159, Jul. 2008.
- **S. Miwa**, and H. Nakajo, A Branch Predictor with Compressed Path Information, In Proceedings of the 2008 Symposium on Advanced Computing Systems and Infrastructures, pp. 255–264, Jun. 2008 (in Japanese).
- K. Ogata, J. Yao, H. Shimada, **S. Miwa**, and S. Tomita, A Dynamic Instruction Scheduler for ALU Cascading, In Proceedings of the 2008 Symposium on Advanced Computing Systems and Infrastructures, pp. 105–114, Jun. 2008 (in Japanese).
- Y. Ogasawara, I. Tate, **S. Miwa** and H. Nakajo, Implementation of a Multi SMT Processor with FPGA, In Proceedings of the 2008 Symposium on Advanced Computing Systems and Infrastructures (poster presentation), pp. 29–30, Jun. 2008 (in Japanese) *(Best Poster Award)*.
- J. Yao, H. Shimada, **S. Miwa**, and S. Tomita, Optimal Pipeline Depth with Pipeline Stage Unification Adoption, In Proceedings of the 2007 International Workshop on Advanced Low Power Systems, pp. 3–9, Jun. 2007.
- T. Yoshimura, K. Saito, H. Shimada, **S. Miwa**, Y. Nakashima, S. Mori, and S. Tomita, Three Quads: An Interconnection Network for Interactive Simulations, In Proceedings of the Asian Simulation Conference 2006, pp. 362–366, Oct. 2006.
- S. Mori, D. Okamura, H. Shimada, **S. Miwa**, Y. Nakashima, and S. Tomita, An FPGA-based Visualization Accelerator: VisA Pro, International Symposium on Advanced Reconfigurable Systems (poster presentation), Dec. 2005.

- T. Fukuyama, M. Fukuda, **S. Miwa**, M. Konishi, M. Goshima, Y. Nakashima, S. Mori, and S. Tomita, Instruction Scheduling with Slack Prediction for Low-Power Processors, In Proceedings of the 2005 Symposium on Advanced Computing Systems and Infrastructures, pp. 123–132, May 2005 (in Japanese).
- T. Tsumura, **S. Miwa**, M. Goshima, and S. Tomita, Neural Network Simulation for Monitoring Memory Architecture, In Proceedings of the 20th Symposium on System Engineering, the Society of Instrument and Control Engineers, pp. 111–114, Feb. 2000 (in Japanese).

Book Chapter

- M. Kondo, I. Miyoshi, K. Inoue, and **S. Miwa**, Power Management Framework for Post-Petascale Supercomputers, Book Chapter in *Advanced Software Technologies for Post-Peta Scale Computing—The Japanese Post-Peta CREST Research Project—* edited by M. Sato, pp. 249–269, Springer, 2018.

Non-refereed Technical Reports

- M. Yuno, H. Yamaki, **S. Miwa**, and H. Honda, Implementation of Video Traffic Inspection Removal on Snort, IEICE Technical Report CPSY-2019-107, pp. 125–130, 2020 (in Japanese).
- Y. Kurokawa, H. Yamaki, **S. Miwa**, and H. Honda, Improving Utilization Efficiency of Caches on Network Devices for High-speed GZIP Decomposition, IEICE Technical Report CPSY-2019-108, pp. 131–136, 2020 (in Japanese).
- S. Yamashita, H. Yamaki, **S. Miwa**, and H. Honda, Reducing Table Lookup Count for High-throughput and Low-energy Internet Routers, IEICE Technical Report IA-2019-58, pp. 57–62, 2019 (in Japanese).
- R. Takakura, H. Yamaki, **S. Miwa**, and H. Honda, Video Flow Non-Mirroring for Reducing NIDS Load Using OpenFlow, IEICE Technical Report IA-2019-57, pp. 51–56, 2019 (in Japanese).
- T. Oyagi, F. Asada, **S. Miwa**, H. Yamaki, and H. Honda, High-Speed Modeling Power of GPU with Consideration of Manufacturing Variation on TSUBAME3.0, IPSJ SIG Technical Report 2019-HPC-172, No. 24, pp. 1–8, 2019 (in Japanese).
- T. Yamazoe, **S. Miwa**, and H. Honda, Real-Time Parallel Processing for Satisfying Per-Main-Key in Sequence Data that Frequently Arrive in an Out-of-Order, IPSJ SIG Technical Report 2019-DBS-169, No. 13, pp. 1–6, 2019 (in Japanese).
- K. Tanaka, H. Yamaki, **S. Miwa**, and H. Honda, Evaluating Pipelining and Port Addition in Packet Processing Caches, IPSJ SIG Technical Report 2019-ARC-237, No. 9, pp. 1–10, 2019 (in Japanese).

- F. Asada, **S. Miwa**, H. Yamaki, and H. Honda, Modeling Variation of GPU Power, The 2019 IEICE General Conference, D-6-15, 2019 (in Japanese).
- Y. Kurokawa, H. Yamaki, **S. Miwa**, and H. Honda, A Technique to Improve Cache Efficiency for GZIP Decode on Network Devices, The 2019 IEICE General Conference, D-6-14, 2019 (in Japanese).
- F. Asada, **S. Miwa**, H. Yamaki, and H. Honda, Modeling Variation of GPU Power, The 2019 IEICE General Conference, D-6-15, 2019 (in Japanese).
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- D. Okamura, Y. Noda, **S. Miwa**, H. Shimada, Y. Nakashima, S. Mori, and S. Tomita, Parallel Volume Rendering with Ultra High Speed Unidirectional Links Composed of DVI, IPSJ SIG Technical Report 2006-SLDM-123, pp. 97–100, 2006 (in Japanese).
- Y. Shinomoto, **S. Miwa**, H. Shimada, Y. Nakashima, S. Mori, and S. Tomita, Improving Texture Access for Volume Rendering on General-Purpose GPU, In Proceedings of Kansai-Section Convention of IPSJ, pp. 187–188, 2005 (in Japanese).
- Y. Shinomoto, **S. Miwa**, H. Shimada, Y. Nakashima, S. Mori, and S. Tomita, Consideration for Speculative Rendering in PVR, IPSJ SIG Technical Report 2005-ARC-164, pp. 145–150, 2005 (in Japanese).
- **S. Miwa**, T. Nagano, M. Goshima, Y. Nakashima, and S. Tomita, Learning Navigation Tasks of Mobile Robots with Recurrent Neural Networks, In Proceedings of Kansai-Section Convention of IPSJ, pp. 181–184, 2003 (in Japanese) *(Student Encouragement Award)*.
- Tsuda, **S. Miwa**, T. Tsumura, M. Goshima, and S. Tomita, Constructing Asynchronous Sequential State Machines with Learning, IEICE Technical Report, CPSY2002-50, pp. 59–64, 2002 (in Japanese).
- **S. Miwa**, A. Tsuda, T. Tsumura, M. Goshima, and S. Tomita, Constructing GSM with Conductance Neural Networks, IEICE Technical Report CPSY2001-40, pp. 39–46, 2001 (in Japanese).
- Tsuda, **S. Miwa**, T. Tsumura, M. Goshima, and S. Tomita, Realizing Sequential Circuit with Conductance Neural Networks, IEICE Technical Report CPSY2001-39, pp. 31–38, 2001 (in Japanese).

Invited Conference Talks

- T. Ono, Y. Kakibuka, N. Jain, A. Bhatele, **S. Miwa**, and K. Inoue, Extending A Network Simulator for Power/Performance Prediction of Large Scale Interconnection Networks,

Modeling and Simulation of HPC Architectures and Applications (the SIAM PP18 Mini-Symposium), Mar. 2018.

- **S. Miwa**, Energy-Efficient Computers with Increased Hardware Resources, the 78th National Convention of Information Processing Society of Japan, Mar. 2016 (in Japanese).
- S. Takeda, H. Noguchi, K. Nomura, S. Fujita, **S. Miwa**, E. Arima, T. Nakada, and H. Nakamura, Low-Power Cache Memory with State-of-the-Art STT-MRAM for High-Performance Processors, the 12th International SoC Design Conference, pp. 153–154, Nov. 2015.
- **S. Miwa**, H. Nakamura, Power Shifting between Networks and CPUs in HPC System, JST/CREST International Symposium on Post Petascale System Software, Dec. 2014.
- M. Kondo, T. Cao, Y. He, Y. Wada, H. Honda, I. Miyoshi, Y. Inadomi, K. Fukazawa, K. Inoue, **S. Miwa**, H. Nakamura, Power Management Framework for Post-Petascale Supercomputers, JST/CREST International Symposium on Post Petescale System Software (Poster Session), Dec. 2014.
- **S. Miwa**, Low-Power Processors in Dark Silicon Era, 2014 Embedded System Symposium, Oct. 2014 (in Japanese).
- H. Nakamura, T. Nakada, **S. Miwa**, (Invited Paper) Normally-Off Computing Project: Challenges and Opportunities, In Proceedings of the 19th Asia and South Pacific Design Automation Conference (ASP-DAC), Special Session 1S-1, pp. 1–5, Jan. 2014.

Invited Colloquium Talks

- Variation of GPU Power in Supercomputing Systems, George Washington University, Washington, DC, USA, Sep. 2019.
- Energy-Efficient Environment for General-Purpose Neural Network Computing, the 2017 New Business Seminar Pioneered by Artificial Intelligence, Minato-ku, Tokyo, Japan, Mar. 2017 (in Japanese).
- Acceleration of Neural Network Computing and its Trend, Triceps Seminar, Chiyoda-ku, Tokyo, Japan, Feb. 2017 (in Japanese).
- Power Management in Supercomputers—Challenges for Post Petascale Computing—, The University of Electro-Communications, Chofu, Tokyo, Japan, Dec. 2015 (in Japanese).
- Network and Memory Power Management in High Performance Computing Systems, IBM Austin Research Labs, Austin, TX, USA, Nov. 2015.
- Heterogeneous CMPs: Low-Power Architectures in Dark Silicon Era, Fujitsu Kawasaki Factory, Kawasaki, Kanagawa, Japan, Apr. 2015 (in Japanese).
- Power Management for Exascale Computing, IBM Austin Research Labs, Austin, TX, USA, Feb. 2014.

Patents

- *Router*, Japan patent pending #2013-111244, 5/27/2013.
- *Converter and conversion method*, Japan patent pending #2010-234673, 10/19/2010.

PROFESSIONAL ACTIVITIES

Track Chair

- IEEE International Symposium on Embedded Multicore/Many-core System-on-Chip (MCSoC), 2018–2020.

Technical Program Committees

- PhD Forum in International Supercomputing Conference (ISC), 2020.
- IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid), 2018–2019.
- International Conference on Parallel Processing (ICPP), 2018.
- International Workshop on Computer Systems and Architectures, 2015–2020.
- International Symposium on Computing and Networking—Across Practical Development and Theoretical Research—, 2013–2020.
- Forum on Information Technology, 2016.
- Annual Meeting on Advanced Computing System and Infrastructure, 2015–2016.
- IEEE International Conference on Computer Design (ICCD), 2014–2015.
- Symposium on Advanced Computing Systems and Infrastructures, 2009–2013.
- National Convention of IPSJ, 2012.

Editorial Boards

- IEICE Transactions on Information and Systems, Apr. 2015–May 2019.
- IPSJ Magazine, Apr. 2010–Mar. 2016.
- IPSJ Transactions on Advanced Computing Systems, Apr. 2011–Mar. 2015, Apr. 2020–Present.
- IPSJ Journal of Information Processing, Jun. 2009–May 2013.

Executive Committees

- SIG of System Architecture, IPSJ, Apr. 2014–Mar. 2017.
- Trax Design Competition, 2016.

External Reviewers

- ACM/EDAC/IEEE Design Automation Conference (DAC), 2014.
- ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2012.
- International Conference for High Performance Computing, Networking, Storage and

Analysis (SC), 2011–2012.

- ACM International Conference on Supercomputing (ICS), 2008.

Others

- Evaluation committee member of Energy-Saving Project, New Energy and Industrial Technology Development Organization, Apr. 2016–Present.
- Representative member of IPSJ, Apr. 2015–Mar. 2016.
- Writing committee member of Knowledge-Base, IEICE, 2011.
- Best Paper Award Selection Working Group of IPSJ, 2009–2010.

JOINED PROJECTS

- Development of Fundamental Technology for Normally-off Computing, IT Innovation Programs, New Energy and Industrial Technology Development Organization, 3,800,000,000 JPY, Oct. 2011–Feb. 2015 (PI: Professor Hiroshi Nakamura).
- Study of Future HPCI Systems with High-Functional and Efficient Latency Cores, Ministry of Education, Culture, Sports and Technology, Japan, 33,533,000 JPY, Oct. 2012–Mar. 2014 (PI: Professor Yutaka Ishikawa).
- Study of Algorithms for Controlling Sensing Data, Hitachi Ltd., 2,300,000 JPY, Dec. 2012–Feb. 2014 (PI: Professor Hiroshi Nakamura).
- Study of Optimizing Architectural Design of Many-core SoC with NoC, Semiconductor Technology Academic Research Center, 17,820,000 JPY, Apr. 2011–Mar. 2013 (PI: Professor Hiroshi Nakamura).
- Demonstration and Evaluation of Ultra Low Power System LSI for ULP Unified Systems, Core Research for Evolutionary Science and Technology, Japan Science and Technology Agency, 9,600,000 JPY, Oct. 2011–Mar. 2013 (PI: Professor Haruhisa Ichikawa).
- Study of Next-Generation Ultra Low Power and High Performance System LSI Using Innovative Power Control, Core Research for Evolutionary Science and Technology, Japan Science and Technology Agency, Apr. 2011–Sep. 2011 (PI: Professor Hiroshi Nakamura).
- Promoting Research on Symbiotic Information Technology for Realization of Information Environment Coordinating with Humans, Grant for Promoting Research on Symbiotic Information Technology, Ministry of Education, Culture, Sports and Technology, Japan, Jan. 2008–Mar. 2011 (PI: Professor Hironori Nakajo).
- Scalable FPGA Systems for Research, Development and Education of Processor Microarchitecture, Academic-Industrial Collaboration of Seeds Innovation, Japan Science and Technology Agency, Dec. 2009–Nov. 2010 (PI: Professor Hironori Nakajo).