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Optimizing Memory Hierarchy within an Internet Router for High-Throughput and Energy-Efficient Packet Processing

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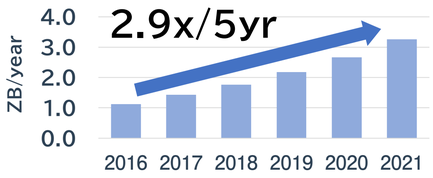
Background

Dramatic increase in network traffic[1]



400Gbps is required for next-generation internet routers

A main challenge towards 400Gbps:

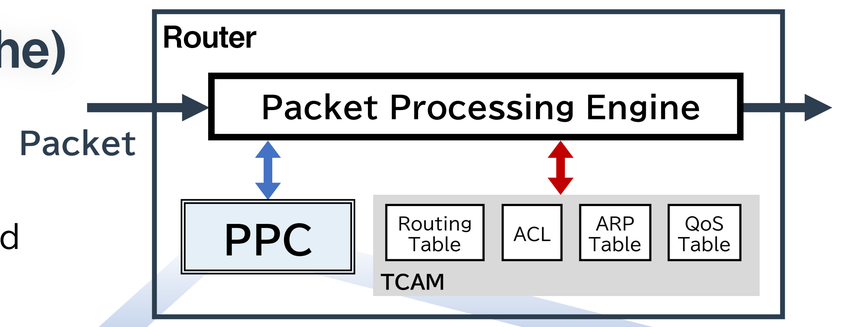
Realize **high-speed table lookup** with small power

Internet routers use low-throughput and power-consuming memory (i.e., TCAM) for table lookup

[1] https://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/complete-white-paper-c11-481360.html

PPC (Packet Processing Cache)

- Reuse results of TCAM lookups
- Reduce the number of TCAM accesses, thereby improving in both throughput and energy efficiency of table lookup (e.g., 215.6 Gbps / 206.3 mW)
- **400Gbps has not yet been achieved**
  - PPC miss rate is **still high** (~18%)
  - Current PPC consists of **only L1 cache**



Flow information (cache tags) — TCAM lookups results

Src IP	Dst IP	Src Port	Dst Port	Proto col	Output I/F	Action	…
10.9.2.3	1.2.3.4	443	65382	TCP	2	Permit	…
10.2.1.4	192.30.0.8	7106	3737	UDP	3	Deny	

13bytes | 15bytes

Objective

No study that optimizes memory hierarchy in routers → Introducing multi-level caches

Experimental Methodology

We evaluate various combinations of L1/L2 PPCs

- Use in-house PPC simulator * + CACTI 6.5
  - * Available at https://github.com/kyontan/cache_simulator
- Use real network traces from [2, 3]
- TCAM params are borrowed from [4]
- Cache configuration
  - Indexed with hashed flow information
  - 4-way set-associative
  - Least Recently Used
  - Write-through
  - Inclusive

[2] http://mawi.wide.ad.jp/
[3] https://labs.ripe.net/
[4] B.Agrawal, et al., TVLSI, 2008

CACTI Parameters	Values
Process technology	32nm
Ports	1 (read) + 1(write)
Transistor models	L1: ITRS-HP, L2: ITRS-LSTP

Throughput and power models

$$Th_{PPC} = L \,/\, \max(t_{L1}, t_{L2} \cdot m_{L1}, t_{TCAM} \cdot m_{L1} \cdot m_{L2})$$

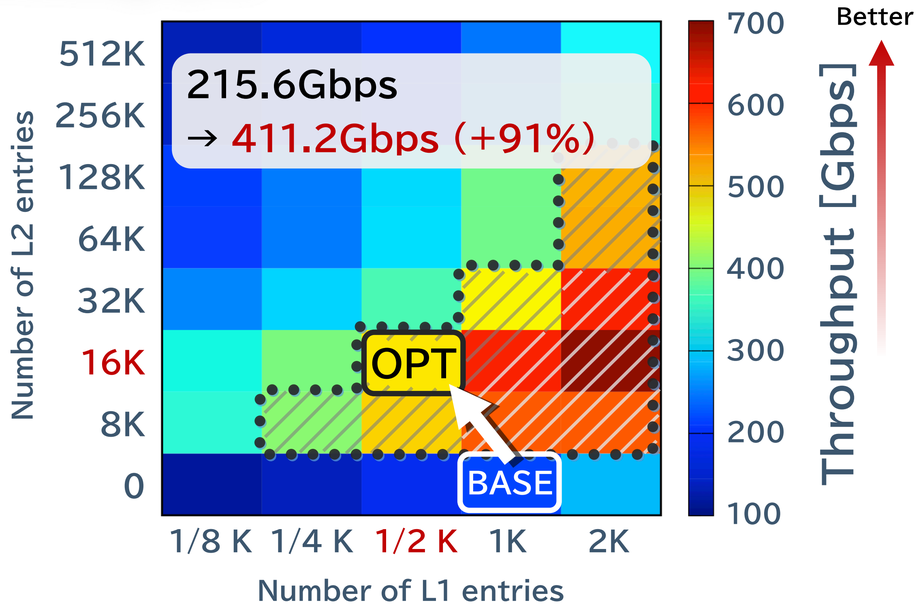
$$P_{PPC} = (DE_{L1} + DE_{L2} \cdot m_{L1} + 4DE_{TCAM} \cdot m_{L1} \cdot m_{L2}) \cdot n + SP_{L1} + SP_{L2} + SP_{TCAM}$$

Variables	Description
Th_{PPC} [bps]	Throughput of PPC
L [bit]	Shortest packet length (=$512bit$)
t_{L1}, t_{L2}, t_{TCAM} [s]	Access latency of L1/L2 PPCs, and TCAM
m_{L1}, m_{L2}	Miss rate of L1/L2 PPCs
P_{PPC} [W]	Average power consumption of PPC
$DE_{L1}, DE_{L2}, DE_{TCAM}$ [J]	Dynamic energy of L1/L2 PPCs and TCAM per access
n [packets/s]	Number of packets per second
$SP_{L1}, SP_{L2}, SP_{TCAM}$ [W]	Static power of L1/L2 PPCs and TCAM

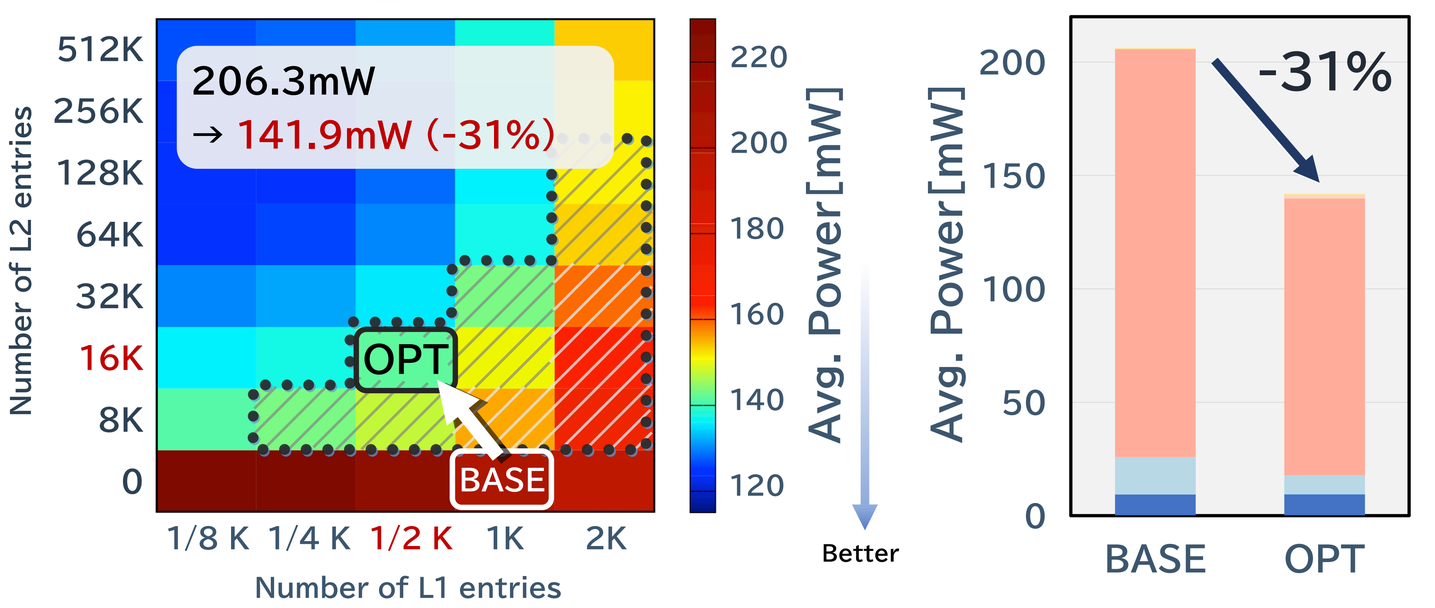
Experimental Result

Throughput

: 400+ Gbps



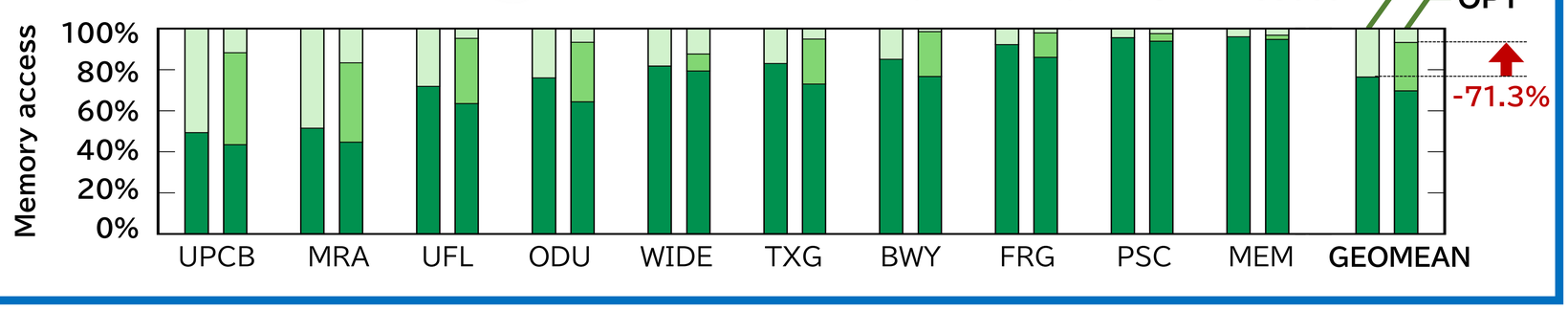
Power consumption



Area

	BASE	OPT
Total [mm²]	90.22	92.76 (+2.8%)
L1 (BASE: 32KB, OPT: 16KB)	0.22	0.16
L2 (512KB)	N/A	2.60
TCAM (2.5MB)	90	90

Breakdown of memory accesses



Conclusion

Introducing L2 PPC and balancing L1/L2 PPCs enable 400Gbps packet processing

Future Work

- Evaluate the impact of 3 and more level PPCs (L3+ PPCs)
- Develop a new insertion policy that uses large caches effectively