Background

Dramatic increase in network traffic[1]

400Gbps is required for next-generation internet routers

A main challenge towards 400Gbps:
Realize high-speed table lookup with small power

PPC (Packet Processing Cache)
- Reuse results of TCAM lookups
- Reduce the number of TCAM accesses, thereby improving in both throughput and energy efficiency of table lookup (e.g., 215.6 Gbps / 206.3 mW)
- 400Gbps has not yet been achieved
  - PPC miss rate is still high (~18%)
  - Current PPC consists of only L1 cache

Objective

No study that optimizes memory hierarchy in routers → Introducing multi-level caches

Experimental Methodology

We evaluate various combinations of L1/L2 PPCs
- Use in-house PPC simulator * + CACTI 6.5
  * Available at [2]
- Use real network traces from [2, 3]
- TCAM params are borrowed from [4]
- Cache configuration
  - Indexed with hashed flow information
  - 4-way set-associative
  - Least Recently Used
  - Write-through
  - Inclusive

Experimental Result

Network traffic

Packet Processing Engine

Throughput and power models

Th_ppc = \frac{L}{\max(t_{L1} \cdot m_{L1} \cdot t_{TCAM} \cdot m_{L2})}

P_{ppc} = (D_{E_{L1}} + D_{E_{L2}} \cdot m_{L1} + 4D_{E_{TCAM}} \cdot m_{L2}) \cdot n + SP_{L1} + SP_{L2} + SP_{TCAM}

Variables

<table>
<thead>
<tr>
<th>Description</th>
<th>Variables</th>
</tr>
</thead>
<tbody>
<tr>
<td>Th_ppc [bps]</td>
<td>L [bit], t_{L1}, t_{L2}, t_{TCAM}, m_{L1}, m_{L2}</td>
</tr>
<tr>
<td>P_{ppc} [W]</td>
<td>D_{E_{L1}}, D_{E_{L2}}, D_{E_{TCAM}} [J], n, SP_{L1}, SP_{L2}, SP_{TCAM}</td>
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</tbody>
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400+ Gbps

Breakdown of memory accesses

Introducing L2 PPC and balancing L1/L2 PPCs enable 400Gbps packet processing

Future Work

- Evaluate the impact of 3 and more level PPCs (L3+ PPCs)
- Develop a new insertion policy that uses large caches effectively

Conclusion